What Is Claimed Is:

1. A method for measuring alignment between a first semiconductor die and a second semiconductor die, comprising:

applying a pattern of voltage signals to a two-dimensional array of conductive transmitter elements that form a transmitter array on the first semiconductor die;

wherein the transmitter array on the first semiconductor die is located over a corresponding two-dimensional array of conductive receiver elements that form a receiver array on the second semiconductor die;

wherein a voltage signal applied to a transmitter element induces a voltage signal in one or more receiver elements;

amplifying voltage signals induced in receiver elements in the receiver array; and

analyzing the amplified signals to determine an alignment between the first semiconductor die and the second semiconductor die.

2. The method of claim 1, wherein transmitter elements have a different spacing than receiver elements, whereby a two-dimensional vernier alignment structure is created when the transmitter array is located over the receiver array.

3. The method of claim 1,

wherein the transmitter array is organized as a two-dimensional $n \times m$ grid including nm conductive elements; and

wherein the receiver array includes at least three conductive elements which are not collinear.

4. The method of claim 1, wherein the receiver array is organized as a two-dimensional $n \times m$ grid including nm conductive elements; and wherein the transmitter array includes at least three conductive elements which are not collinear.

5. The method of claim 1, wherein determining the alignment involves determining six degrees of alignment, including:

an x alignment parallel to plane of the receiver array;

a y alignment parallel to plane of the receiver array and normal to the x axis;

a z alignment normal to the plane of the receiver array;

an angular alignment, θ, about the z axis;

an angular alignment, Ψ, about the y axis; and

an angular alignment, Φ, about the x axis.

6. The method of claim 5, wherein determining the alignment involves analyzing coupling capacitances between individual receiver elements and individual transmitter elements to determine the x alignment, the y alignment and the angular alignment, θ.

7. The method of claim 6, wherein analyzing the coupling capacitances involves determining a nearest neighbor mapping between receiver elements and transmitter elements.

8. The method of claim 5, wherein determining the alignment involves using a mapping function generated by a three-dimensional capacitance field solver simulation to determine the z alignment, the angular alignment, Ψ, and the angular alignment, Φ.

9. The method of claim 5, wherein determining the z alignment, the angular alignment, Ψ, and the angular alignment, Φ, involves summing capacitances between individual receiver elements in the receiver array and all transmitter elements in the transmitter array, thereby effectively considering the transmitter array to be one large plate.

10. The method of claim 5, wherein determining the z alignment, the angular alignment, Ψ, and the angular alignment, Φ, involves summing capacitances between individual transmitter elements in the transmitter array and all receiver elements in the receiver array, thereby effectively considering the receiver array to be one large plate.

11. The method of claim 1, further comprising electrically varying the pitch of the transmitter array by grouping together adjacent transmitter elements.

12. The method of claim 1, further comprising electrically varying the pitch of the receiver array by grouping together adjacent receiver elements.

13. The method of claim 1, wherein transmitter elements and receiver elements are:

square;

rectangular;

hexagonal;
triangular;
oval; or
round.

14. The method of claim 1,

wherein transmitter elements are located in a metal layer of the first semiconductor die and are not covered by higher layers of metal; and

wherein receiver elements are located in a metal layer of the second semiconductor die and are not covered by higher layers of metal.

15. An apparatus that measures alignment between a first semiconductor die and a second semiconductor die, comprising:

a two-dimensional array of conductive transmitter elements that form a transmitter array on the first semiconductor die;

a two-dimensional array of conductive receiver elements that form a receiver array on the second semiconductor die;

a driving mechanism configured to apply a pattern of voltage signals to the transmitter array;

wherein a voltage signal applied to a transmitter element induces a voltage signal in one or more receiver elements when the transmitter array is located over the receiver array;

an amplification mechanism configured to amplify voltage signals induced in receiver elements in the receiver array; and

an analysis mechanism configured to analyze the amplified signals to determine an alignment between the first semiconductor die and the second semiconductor die.

16. The apparatus of claim 15, wherein transmitter elements have a different spacing than receiver elements, whereby a two-dimensional vernier alignment structure is created when the transmitter array is located over the receiver array.

17. The apparatus of claim 15,

wherein the transmitter array is organized as a two-dimensional $n \times m$ grid including nm conductive elements; and

wherein the receiver array includes at least three conductive elements which are not collinear.

18. The apparatus of claim 15,

wherein the receiver array is organized as a two-dimensional $n \times m$ grid including nm conductive elements; and

wherein the transmitter array includes at least three conductive elements which are not collinear.

19. The apparatus of claim 15, wherein the driving mechanism and the analysis mechanism are configured to determine six degrees of alignment, including:

an x alignment parallel to plane of the receiver array;

a y alignment parallel to plane of the receiver array and normal to the x axis;

a z alignment normal to the plane of the receiver array;

an angular alignment, θ, about the z axis;

an angular alignment, Ψ, about the y axis; and

an angular alignment, Φ, about the x axis.

20. The apparatus of claim 19, wherein the analysis mechanism is configured to determine coupling capacitances between individual receiver elements and individual transmitter elements to determine the x alignment, the y alignment and the angular alignment, θ.

21. The apparatus of claim 20, wherein the analysis mechanism is configured to determine a nearest neighbor mapping between receiver elements and transmitter elements.

22. The apparatus of claim 19, wherein the analysis mechanism is configured to use a mapping function generated by a three-dimensional capacitance field solver simulation to determine the z alignment, the angular alignment, Ψ, and the angular alignment, Φ.

23. The apparatus of claim 19, wherein the apparatus is configured to determine the z alignment, the angular alignment, Ψ, and the angular alignment, Φ, by summing capacitances between individual receiver elements in the receiver array and all transmitter elements in the transmitter array, thereby effectively considering the transmitter array to be one large plate.

24. The apparatus of claim 19, wherein the apparatus is configured to determine the z alignment, the angular alignment, Ψ, and the angular alignment, Φ, by summing capacitances between individual transmitter elements in the transmitter array and all receiver elements in the receiver array, thereby effectively considering the receiver array to be one large plate.

25. The apparatus of claim 15, wherein the apparatus is configured to electrically vary the pitch of the transmitter array by grouping together adjacent transmitter elements.

26. The apparatus of claim 15, wherein the apparatus is configured to electrically vary the pitch of the receiver array by grouping together adjacent receiver elements.

27. The apparatus of claim 15, wherein transmitter elements and receiver elements are:

square;
rectangular;
hexagonal;
triangular;
oval; or
round.

28. The apparatus of claim 15,

wherein transmitter elements are located in a metal layer of the first semiconductor die and are not covered by higher layers of metal; and

wherein receiver elements are located in a metal layer of the second semiconductor die and are not covered by higher layers of metal.